Multicell Battery Gas Gauge with Temperature, Voltage and Current Measurement

FEATURES

- **Measures Accumulated Battery Charge and Discharge**
- **3.6V to 20V Operating Range for Multiple Cells Application**
- **14-Bit ADC Measures Voltage, Current and Temperature**
- **1% Voltage, Current and Charge Accuracy**
- ±50mV Sense Voltage Range
- High Side Sense
- General Purpose Measurements for Any Battery Chemistry and Capacity
- I²C/SMBus Interface
- Configurable Alert Output/Charge Complete Input
- Quiescent Current Less Than 120µA
- Small 8-Lead 3mm × 3mm DFN Package

APPLICATIONS

- Power Tools
- Electric Bicycles
- Portable Medical Equipment
- Video Cameras

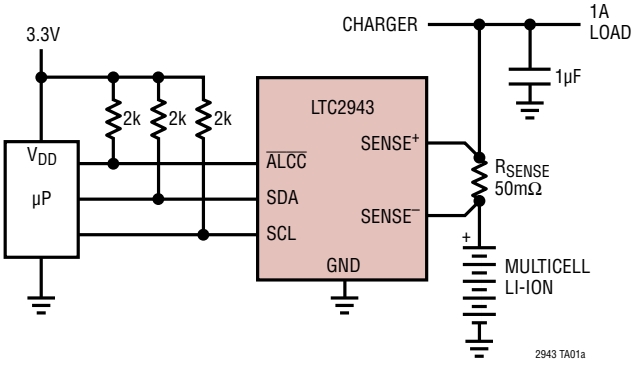
DESCRIPTION

The LTC®2943 measures battery charge state, battery voltage, battery current and its own temperature in portable product applications. The wide input voltage range allows use with multicell batteries up to 20V. A precision coulomb counter integrates current through a sense resistor between the battery's positive terminal and the load or charger. Voltage, current and temperature are measured with an internal 14-bit No Latency ΔΣ™ ADC. The measurements are stored in internal registers accessible via the onboard I²C/SMBus Interface.

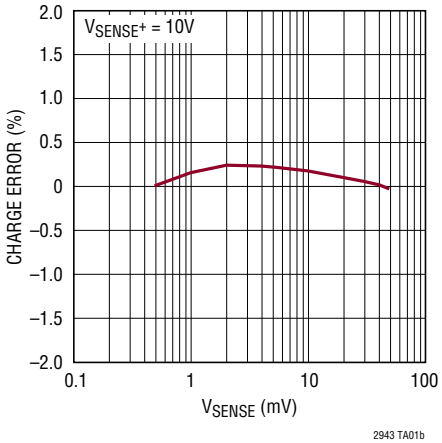
The LTC2943 features programmable high and low thresholds for all four measured quantities. If a programmed threshold is exceeded, the device communicates an alert using either the SMBus alert protocol or by setting a flag in the internal status register. The LTC2943 requires only a single low value sense resistor to set the measured current range.

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TYPICAL APPLICATION



Total Charge Error vs Differential Sense Voltage

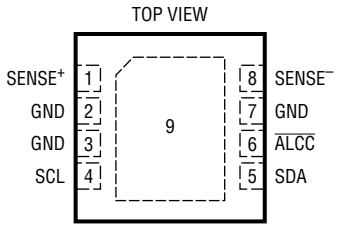


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (SENSE+) ..... –0.3V to 24V
SCL, SDA, $\overline{ALCC}$ Voltage ..... –0.3V to 6V
SENSE– ..... (–0.3V + V_{SENSE}^+) to (V_{SENSE}^+ + 0.3V)
Operating Ambient Temperature Range
LTC2943C ..... 0°C to 70°C
LTC2943I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JA} = 100°C/W
EXPOSED PAD (PIN 9) PCB GND CONNECTION OPTIONAL

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2943CDD#PBF	LTC2943CDD#TRPBF	LGCS	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2943IDD#PBF	LTC2943IDD#TRPBF	LGCS	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Requirements							
V_{SENSE}^+	Supply Voltage			3.6		20	V
I_{SUPPLY}	Supply Current (Note 3)	Battery Gas Gauge On, ADC Sleep Battery Gas Gauge On, ADC On Shutdown	● ● ●		80 650 15	120 750 25	µA µA µA
I_{SENSE}^+	Pin Current (Note 3)	Battery Gas Gauge On, ADC Sleep Battery Gas Gauge On, ADC On Shutdown			80 500 15		µA µA µA
I_{SENSE}^-	Pin Current (Note 3)	Battery Gas Gauge On, ADC Sleep Battery Gas Gauge On, ADC On Shutdown			1 150 1		µA µA µA
V_{UVLO}	Undervoltage Lockout Threshold	V_{SENSE}^+ Falling	●	3.0	3.3	3.6	V
Coulomb Counter							
V_{SENSE}	Sense Voltage Differential Input Range	$V_{SENSE}^+ – V_{SENSE}^-$	●			±50	mV
R_{IDR}	Differential Input Resistance Across SENSE+ and SENSE– (Note 8)				400		kΩ
q_{LSB}	Charge LSB (Note 4)	Prescaler M = 4096(Default), R_{SENSE} = 50mΩ			0.340		mAh

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
TCE	Total Charge Error (Note 5)	10mV ≤ $\|V_{SENSE}\|$ ≤ 50mV DC 10mV ≤ $\|V_{SENSE}\|$ ≤ 50mV DC 1mV ≤ $\|V_{SENSE}\|$ ≤ 10mV DC (Note 8)	 ● ●			±1 ±1.5 ±3.5	% % %
V_{OSE}	Effective Differential Offset Voltage (Note 9)	V_{SENSE} ≥ 500µV, V_{SENSE}^+ = 10V	●		5	10	µV
Voltage Measurement ADC							
	Resolution (No Missing Codes)	(Note 8)	●	14			Bits
$V_{FS(V)}$	Full-Scale Voltage Conversion				23.6		V
ΔV_{LSB}	Quantization Step of 14-Bit Voltage ADC	(Note 6)			1.44		mV
TUE_V	Voltage Total Unadjusted Error		 ●			1 1.3	% %
$Gain_V$	Voltage Gain Accuracy		●			1.3	%
INL_V	Integral Nonlinearity	V_{SENSE}^+ > 5V	●		±1	±4	LSB
		3.6V ≤ V_{SENSE}^+ ≤ 5V	●			±8	LSB
$T_{CONV(V)}$	Voltage Conversion Time		●			48	ms
Current Measurement ADC							
	Resolution (No Missing Codes)	(Note 8)	●	12			Bits
$V_{FS(I)}$	Full-Scale Current Conversion		●		±60		mV
V_{SENSE}	Sense Voltage Differential Input Range	$V_{SENSE}^+ - V_{SENSE}^-$	●			±50	mV
ΔI_{LSB}	Quantization Step of 12-Bit Current ADC	(Note 6)			29.3		µV
$Gain_I$	Current Gain Accuracy		 ●			1 1.3	% %
$V_{OS(I)}$	Offset				±1	±10	LSB
INL_I	Integral Nonlinearity		●		±1	±4	LSB
$T_{CONV(I)}$	Current Conversion Time		●			8	ms
Temperature Measurement ADC							
	Resolution (No Missing Codes)	(Note 8)	●	11			Bits
T_{FS}	Full-Scale Temperature				510		K
ΔT_{LSB}	Quantization Step of 11-Bit Temperature ADC	(Note 6)			0.25		K
TUE_T	Temperature Total Unadjusted Error	V_{SENSE}^+ ≥ 5V (Note 8)	 ●			±3 ±5	K K
$T_{CONV(T)}$	Temperature Conversion Time		●			8	ms
Digital Inputs and Digital Outputs							
$V_{ITH(HV)}$	Logic Input Threshold	V_{SENSE}^+ ≥ 5V	●	0.8		2.2	V
$V_{ITH(LV)}$		3.6V < V_{SENSE}^+ < 5V		0.5		1.8	V
V_{OL}	Low Level Output Voltage, $\overline{ALCC}$, SDA	I = 3mA, V_{SENSE}^+ ≥ 5V	●			0.4	V
I_{IN}	Input Leakage, $\overline{ALCC}$, SCL, SDA	V_{IN} = 5V	●			1	µA
C_{IN}	Input Capacitance, $\overline{ALCC}$, SCL, SDA	(Note 8)	●			10	pF

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{PCC}	Minimum Charge Complete ($\overline{CC}$) Pulse Width					1	µs
I²C Timing Characteristics							
$f_{SCL(MAX)}$	Maximum SCL Clock Frequency		●	400	900		kHz
$t_{BUF(MAX)}$	Bus Free Time Between Stop/Start		●			1.3	µs
$t_{SU(STA(MIN))}$	Minimum Repeated Start Set-Up Time		●			600	ns
$t_{HD(STA(MIN))}$	Minimum Hold Time (Repeated) Start Condition		●			600	ns
$t_{SU(STO(MIN))}$	Minimum Set-Up Time for Stop Condition		●			600	ns
$t_{SU(DAT(MIN))}$	Minimum Data Setup Time Input		●			100	ns
$T_{HD(DAT(MIN))}$	Minimum Data Hold Time Input		●			50	ns
T_{HDDATO}	Data Hold Time Input Output		●	0.3		0.9	µs
T_{OF}	Data Output Fall Time	(Notes 7, 8)	●	20 + 0.1 • C_B		300	ns

Note 1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2. All currents into pins are positive, all voltages are referenced to GND unless otherwise specified.

Note 3. $I_{SUPPLY} = I_{SENSE^+} + I_{SENSE^-}$. In most operating modes, I_{SUPPLY} is flowing in $SENSE^+$ pin. Only during ADC conversions, current is flowing in $SENSE^-$ pin as well. Typically, $I_{SENSE^-} = V_{SENSE^-}/150k$ during ADC voltage conversion and I_{SENSE^-} = 20µA during ADC current conversion.

Note 4. The equivalent charge of an LSB in the accumulated charge register depends on the value of R_{SENSE} and the setting of the internal prescaling factor M:

$q_{LSB} = 0.340mAh \bullet (50m\Omega/R_{SENSE}) \bullet (M/4096)$

See Choosing R_{SENSE} and Choosing Coulomb Counter Prescaler M section for more information. 1mAh = 3.6C (Coulombs)

Note 5. Deviation of q_{LSB} from its nominal value.

Note 6. The quantization step of the 12-bit ADC in current mode and 11-bit ADC in temperature mode is not the same as the LSB of the combined 16-bit voltage registers (O, P) and 16-bit temperature registers (U, V). See Voltage, Current and Temperature Registers section for more information.

Note 7. C_B = Capacitance of one bus line in pF (10pF ≤ C_B ≤ 400pF).

Note 8. Guaranteed by design, not subject to test.

Note 9. See Effect of Differential Offset Voltage on Total Charge Error section.

TIMING DIAGRAM

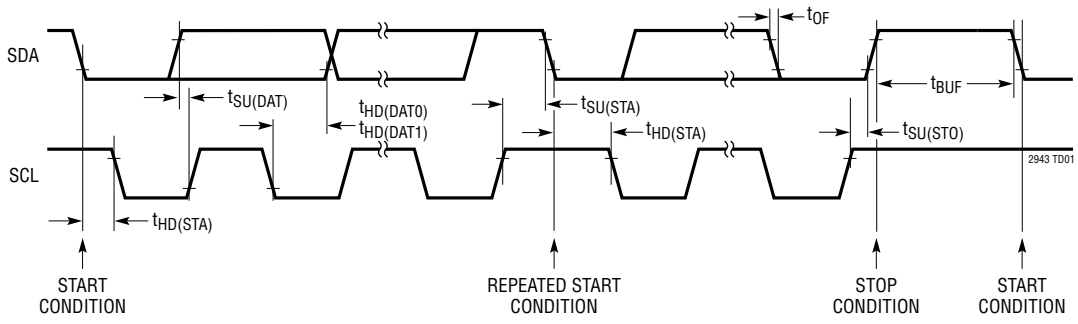
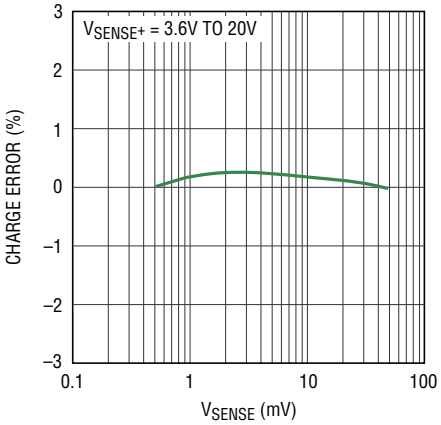


Figure 1. Definition of Timing on I²C Bus

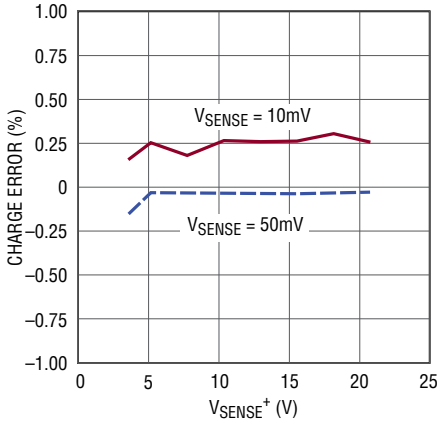
TYPICAL PERFORMANCE CHARACTERISTICS

Total Charge Error vs Differential Sense Voltage



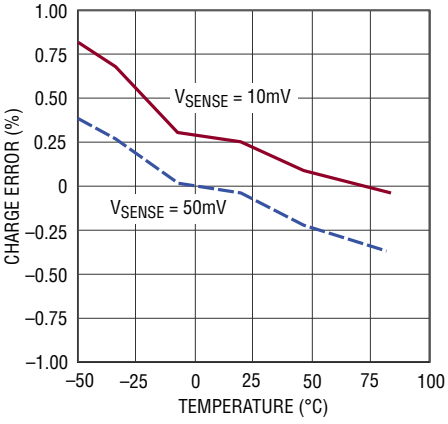
2943 G01

Total Charge Error vs Supply Voltage



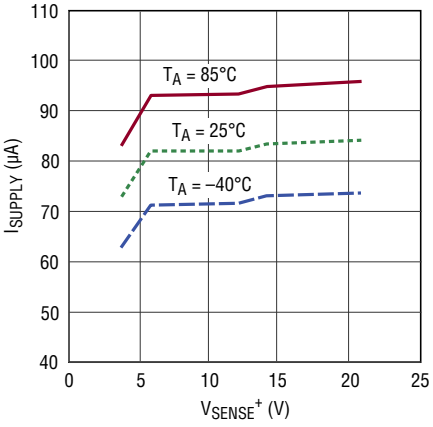
2943 G02

Total Charge Error vs Temperature



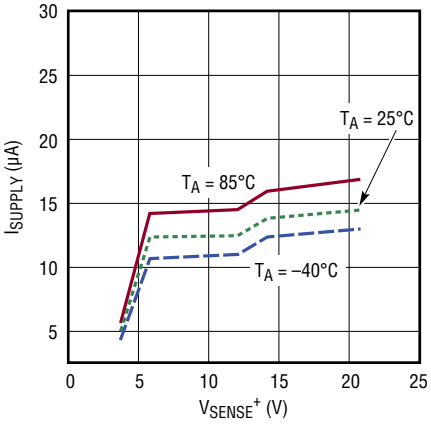
2943 G03

Supply Current vs Supply Voltage



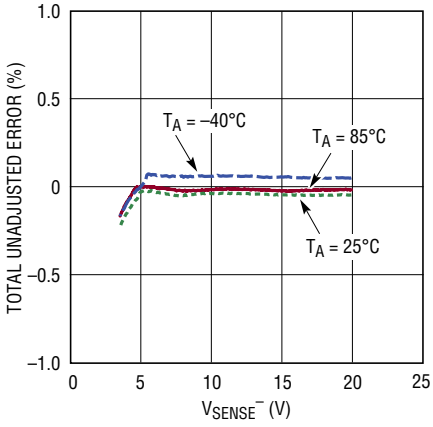
2943 G04

Shutdown Supply Current vs Supply Voltage



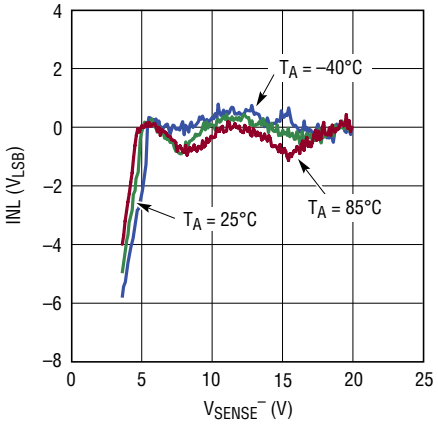
2943 G05

Voltage Measurement ADC Total Unadjusted Error



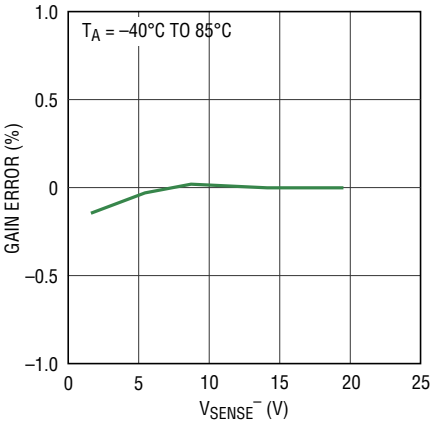
2943 G06

Voltage Measurement ADC Integral Nonlinearity



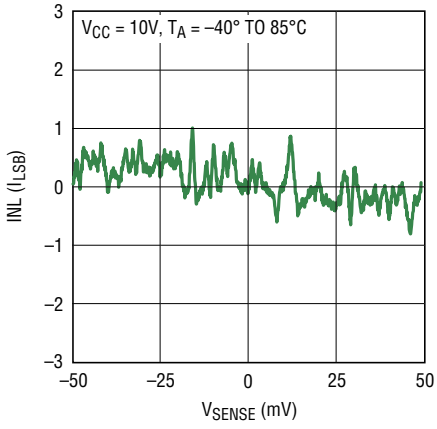
2944 G07

Current Measurement ADC Gain Error



2943 G08

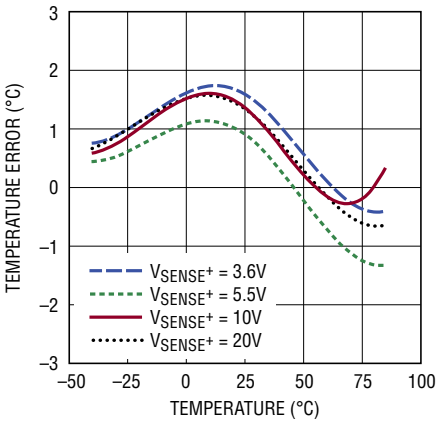
Current Measurement ADC Integral Nonlinearity



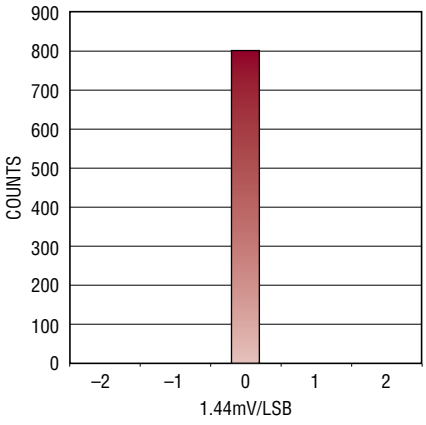
2943 G09

TYPICAL PERFORMANCE CHARACTERISTICS

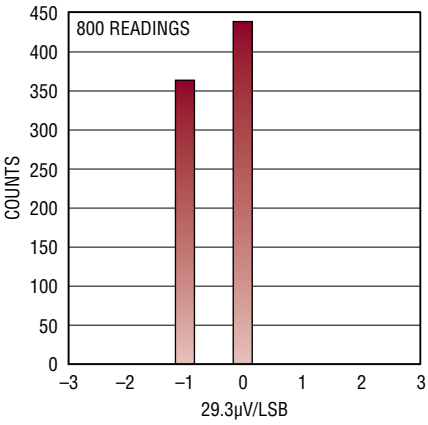
Temperature Error vs Temperature



Voltage Measurements Noise



Current Measurements Noise



PIN FUNCTIONS

SENSE+ (Pin 1): Positive Current Sense Input and Power Supply. Connect to load/charger side of the sense resistor. V_{SENSE^+} operating range is 3.6V to 20V. SENSE+ is also an input to the ADC during current measurement. Bypass to GND with a 1µF capacitor located as close to pin 1 and pin 2 as possible.

GND (Pin 2, Pin 3, Pin 7): Device Ground. Connect directly to the negative battery terminal.

SCL (Pin 4): Serial Bus Clock Input.

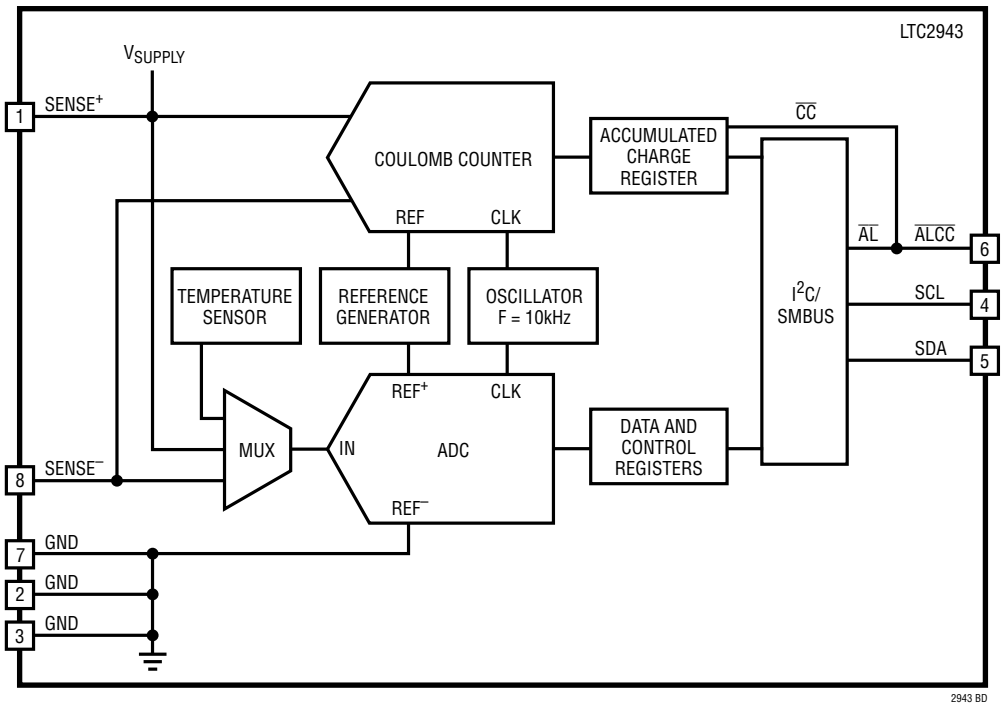
SDA (Pin 5): Serial Bus Data Input and Output.

$\overline{\text{ALCC}}$ (Pin 6): Alert Output or Charge Complete Input. Configured either as an SMBus alert output or charge complete input by control register bits B[2:1]. At power-up, the pin defaults to alert mode conforming to the SMBus alert response protocol. It behaves as an open-drain logic output that pulls to GND when any threshold register value is exceeded. When configured as a charge complete input, connect to the charge complete output from the battery charger circuit. A low level at $\overline{\text{CC}}$ sets the value of the accumulated charge (registers C, D) to FFFFh.

SENSE– (Pin 8): Negative Current Sense Input. Connect SENSE– to the positive battery terminal side of the sense resistor. The voltage between SENSE– and SENSE+ must remain within ±50mV in normal operation. SENSE– is also an input to the ADC during voltage and current measurement.

Exposed Pad (Pin 9): Exposed pad may be left open or connected to device ground (GND).

BLOCK DIAGRAM



OPERATION

Overview

The LTC2943 is a battery gas gauge designed for use with multicell batteries with terminal voltages from 3.6V to 20V. It measures battery charge and discharge, battery voltage, current and its own temperature.

A precision analog coulomb counter integrates current through a sense resistor between the battery's positive terminal and the load or charger. Battery voltage, battery current and silicon temperature are measured with an internal ADC.

Coulomb Counter

Charge is the time integral of current. The LTC2943 measures charge by monitoring the voltage developed across a sense resistor. The differential voltage between SENSE$^+$ and SENSE$^-$ is applied to an auto-zeroed differential analog integrator to infer charge.

When the integrator output ramps to REFHI or REFLO levels, switches S1, S2, S3 and S4 toggle to reverse the ramp direction (Figure 2). By observing the condition of the switches and the ramp direction, polarity is determined. This approach also significantly lowers the impact on offset of the analog integrator as described in the Differential Offset Voltage section.

A programmable prescaler effectively increases integration time by a factor M programmable from 1 to 4096. At each underflow or overflow of the prescaler, the accumulated charge register (ACR) value is incremented or decremented one count. The value of accumulated charge is read via the I^{2}C interface.

Voltage, Current and Temperature ADC

The LTC2943 includes a 14-bit No Latency ΔΣ analog-to-digital converter, with internal clock and voltage reference circuits.

The ADC can be used to monitor the battery voltage at SENSE$^-$ or the battery current flowing through the sense resistor or to convert the output of the on-chip temperature sensor.

Conversion of voltage, current and temperature are triggered by programming the control register via the I^{2}C interface. The LTC2943 includes a scan mode where voltage, current and temperature conversion measurements are executed every 10 seconds. At the end of each conversion the corresponding registers are updated and the converter goes to sleep to minimize quiescent current.

The temperature sensor generates a voltage proportional to temperature with a slope of 2mV/K resulting in a voltage of 600mV at 27°C.

Power-Up Sequence

When SENSE$^+$ rises above a threshold of approximately 3.3V, the LTC2943 generates an internal power-on reset (POR) signal and sets all registers to their default state. In the default state, the coulomb counter is active while the voltage, current and temperature ADC is switched off. The accumulated charge register is set to mid-scale (7FFFh), all low threshold registers are set to 0000h and all high threshold registers are set to FFFFh. The alert mode is enabled and the coulomb counter prescaling factor M is set to 4096.

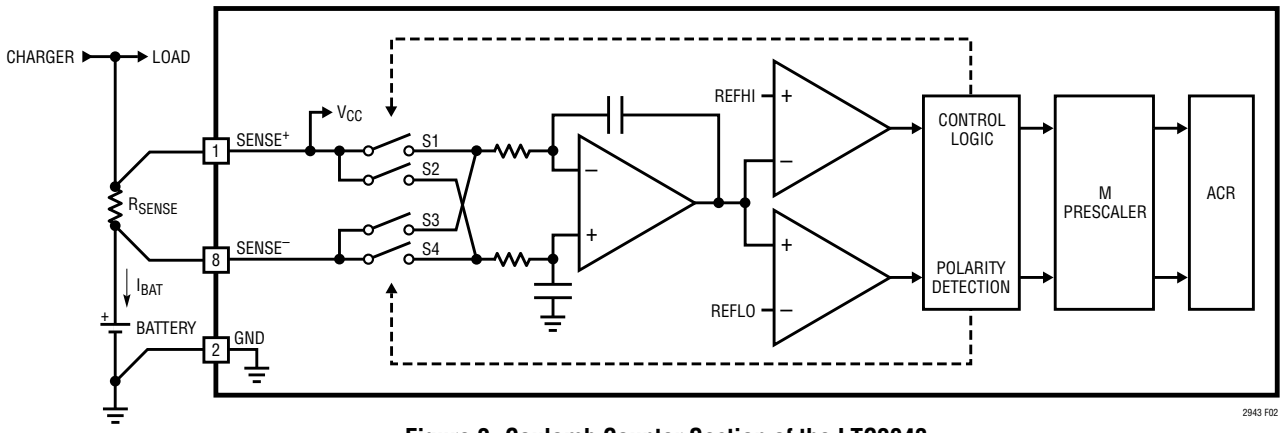


Figure 2. Coulomb Counter Section of the LTC2943

APPLICATIONS INFORMATION

Internal Registers

The LTC2943 register map is shown in Table 1. The LTC2943 integrates current through a sense resistor, measures battery voltage, current and temperature and stores the results in internal 16-bit registers accessible via I^2C. High and low limits can be programmed for each measured quantity. The LTC2943 continuously monitors these limits and sets a flag in the status register when a limit is exceeded. If the alert mode is enabled, the $\overline{ALCC}$ pin pulls low.

Table 1. Register Map

ADDRESS	NAME	REGISTER DESCRIPTION	R/W	DEFAULT
00h	A	Status	R	See Table 2
01h	B	Control	R/W	3Ch
02h	C	Accumulated Charge MSB	R/W	7Fh
03h	D	Accumulated Charge LSB	R/W	FFh
04h	E	Charge Threshold High MSB	R/W	FFh
05h	F	Charge Threshold High LSB	R/W	FFh
06h	G	Charge Threshold Low MSB	R/W	00h
07h	H	Charge Threshold Low LSB	R/W	00h
08h	I	Voltage MSB	R	00h
09h	J	Voltage LSB	R	00h
0Ah	K	Voltage Threshold High MSB	R/W	FFh
0Bh	L	Voltage Threshold High LSB	R/W	FFh
0Ch	M	Voltage Threshold Low MSB	R/W	00h
0Dh	N	Voltage Threshold Low LSB	R/W	00h
0Eh	O	Current MSB	R	00h
0Fh	P	Current LSB	R	00h
10h	Q	Current Threshold High MSB	R/W	FFh
11h	R	Current Threshold High LSB	R/W	FFh
12h	S	Current Threshold Low MSB	R/W	00h
13h	T	Current Threshold Low LSB	R/W	00h
14h	U	Temperature MSB	R	00h
15h	V	Temperature LSB	R	00h
16h	W	Temperature Threshold High	R/W	FFh
17h	X	Temperature Threshold Low	R/W	00h

R = Read, W = Write

The status of the charge, voltage, current and temperature alerts is reported in the status register shown in Table 2.

Table 2. Status Register (A)

BIT	NAME	OPERATION	DEFAULT
A[7]	Reserved		
A[6]	Current Alert	Indicates one of the current limits was exceeded	0
A[5]	Accumulated Charge Overflow/ Underflow	Indicates that the value of the ACR hit either top or bottom	0
A[4]	Temperature Alert	Indicates one of the temperature limits was exceeded	0
A[3]	Charge Alert High	Indicates that the ACR value exceeded the charge threshold high limit	0
A[2]	Charge Alert Low	Indicates that the ACR value exceeded the charge threshold low limit	0
A[1]	Voltage Alert	Indicates one of the voltage limits was exceeded	0
A[0]	Undervoltage Lockout Alert	Indicates recovery from undervoltage. If set to 1, a UVLO has occurred and the contents of the registers are uncertain	1

After each voltage, current or temperature conversion, the conversion result is compared to the respective threshold registers. If a value in the threshold registers is exceeded, the corresponding bit A[6], A[4] or A[1] is set.

The accumulated charge register (ACR) is compared to the charge thresholds every time the analog integrator increments or decrements the prescaler. If the ACR value exceeds the threshold register values, the corresponding bit A[3] or A[2] are set. Bit A[5] is set if the accumulated charge registers (ACR) overflows or underflows. At each overflow or underflow, the ACR rolls over and resumes integration.

The undervoltage lockout (UVLO) bit of the status register A[0] is set if, during operation, the voltage on the $SENSE^+$ pin drops below 3.5V without reaching the POR level. The analog parts of the coulomb counter are switched off while the digital register values are retained. After recovery of the supply voltage the coulomb counter resumes integrating with the stored value in the accumulated charge registers but it has missed any charge flowing while $SENSE^+ < 3.5V$.

APPLICATIONS INFORMATION

All status register bits are cleared after being read by the host, but might be reasserted after the next temperature, voltage or current conversion or charge integration, if the corresponding alert condition is still fulfilled.

Control Register (B)

The operation of the LTC2943 is controlled by programming the control register. Table 3 shows the organization of the 8-bit control register B[7:0].

Table 3. Control Register B

BIT	NAME	OPERATION	DEFAULT
B[7:6]	ADC Mode	[11] Automatic Mode: continuously performing voltage, current and temperature conversions [10] Scan Mode: performing voltage, current and temperature conversion every 10s [01] Manual Mode: performing single conversions of voltage, current and temperature then sleep [00] Sleep	[00]
B[5:3]	Prescaler M	Sets coulomb counter prescaling factor M between 1 and 4096. Default is 4096. Maximum value is limited to 4096	[111]

B[5:3]	M
000	1
001	4
010	16
011	64
100	256
101	1024
110	4096
111	4096

BIT	NAME	OPERATION	DEFAULT
B[2:1]	$\overline{\text{ALCC}}$ Configure	Configures the $\overline{\text{ALCC}}$ pin. [10] Alert Mode. Alert functionality enabled. Pin becomes logic output. [01] Charge Complete Mode. Pin becomes logic input and accepts charge complete inverted signal (e.g., from a charger) to set accumulated charge register (C,D) to FFFFh. [00] $\overline{\text{ALCC}}$ pin disabled. [11] Not allowed.	[10]
B[0]	Shutdown	Shut down analog section to reduce I_{SUPPLY}.	[0]

Power Down B[0]

Setting B[0] to 1 shuts down the analog parts of the LTC2943, reducing the current consumption to less than 15µA (typical). The circuitry managing I^2C communication remains operating and the values in the registers are retained. Note that any charge flowing while B[0] is 1 is not measured and any charge information below 1LSB of the accumulated charge register is lost.

Alert/Charge Complete Configuration B[2:1]

The $\overline{\text{ALCC}}$ pin is a dual function pin configured by the control register. By setting bits B[2:1] to [10] (default), the $\overline{\text{ALCC}}$ pin is configured as an alert pin following the SMBus protocol. In this configuration, the $\overline{\text{ALCC}}$ is pulled low if one of the four measured quantities (charge, voltage, current, temperature) exceeds its high or low threshold or if the value of the accumulated charge register overflows or underflows. An alert response procedure started by the master resets the alert at the $\overline{\text{ALCC}}$ pin. If the configuration of the $\overline{\text{ALCC}}$ pin is changed while it is pulled low due to an alert condition, the part will continue to pull $\overline{\text{ALCC}}$ low until a successful alert response procedure (ARA) has been issued by the master. For further information see the Alert Response Protocol section.

Setting the control bits B[2:1] to [01] configures the $\overline{\text{ALCC}}$ pin as a digital input. In this mode, a low input on the $\overline{\text{ALCC}}$ pin indicates to the LTC2943 that the battery is full and the accumulated charge register is set to its maximum, value FFFFh.

APPLICATIONS INFORMATION

If neither the alert nor the charge complete functionality is desired, bits B[2:1] should be set to [00]. The $\overline{ALCC}$ pin is then disabled and should be tied to the supply of the I^2C bus with a 10k resistor.

Avoid setting B[2:1] to [11] as it enables the alert and the charge complete modes simultaneously.

Choosing R_{SENSE}

To achieve the specified precision of the coulomb counter, the differential voltage between $SENSE^+$ and $SENSE^-$ must stay within ±50mV. With input signals up to 300mV the LTC2943 will remain functional but the precision of the coulomb counter is not guaranteed.

The required value of the external sense resistor, R_{SENSE}, is determined by the maximum input range of V_{SENSE} and the maximum current of the application:

$$R_{SENSE} \leq \frac{50mV}{I_{MAX}}$$

The choice of the external sense resistor value influences the gain of the coulomb counter. A larger sense resistor gives a larger differential voltage between $SENSE^+$ and $SENSE^-$ for the same current resulting in more precise coulomb counting. The amount of charge represented by the least significant bit (q_{LSB}) of the accumulated charge (registers C, D) is equal to:

$$q_{LSB} = 0.340mAh \bullet \frac{50m\Omega}{R_{SENSE}} \bullet \frac{M}{4096}$$

or

$$q_{LSB} = 0.340mAh \bullet \frac{50m\Omega}{R_{SENSE}}$$

when the prescaler is set to its default value of M = 4096.

Note that 1mAh = 3.6C (coulomb).

Choosing $R_{SENSE} = 50mV/I_{MAX}$ is not sufficient in applications where the battery capacity (Q_{BAT}) is very large compared to the maximum current (I_{MAX}):

$$Q_{BAT} > I_{MAX} \bullet 22\,Hours$$

For such low current applications with a large battery, choosing R_{SENSE} according to $R_{SENSE} = 50mV/I_{MAX}$ can lead to a q_{LSB} smaller than $Q_{BAT}/2^{16}$ and the 16-bit accumulated charge register may underflow before the battery is exhausted or overflow during charge. Choose, in this case, a maximum R_{SENSE} of:

$$R_{SENSE} \leq \frac{0.340mAh \bullet 2^{16}}{Q_{BAT}} \bullet 50m\Omega$$

In an example application where the maximum current is I_{MAX} = 100mA, calculating $R_{SENSE} = 50mV/I_{MAX}$ would lead to a sense resistor of 500mΩ. This gives a q_{LSB} of 34µAh and the accumulated charge register can represent a maximum battery capacity of Q_{BAT} = 34µAh•65535 = 2228mAh. If the battery capacity is larger, R_{SENSE} must be lowered. For example, R_{SENSE} should be reduced to 150mΩ if a battery with a capacity of 7200mAh is used.

Choosing Coulomb Prescaler M B[5:3]

If the battery capacity (Q_{BAT}) is small compared to the maximum current (I_{MAX}) the prescaler value M should be changed from its default value (4096).

In these applications with a small battery but a high maximum current, q_{LSB} can get quite large with respect to the battery capacity. For example, if the battery capacity is 100mAh and the maximum current is 1A, the standard equation leads to choosing a sense resistor value of 50mΩ, resulting in:

$$q_{LSB} = 0.340mAh = 1224mC$$

The battery capacity then corresponds to only 294 q_{LSB} and less than 0.5% of the accumulated charge register is utilized.

To preserve digital resolution in this case, the LTC2943 includes a programmable prescaler. Lowering the prescaler factor M reduces q_{LSB} to better match the accumulated charge register to the capacity of the battery. The prescaling factor M can be chosen between 1 and its default value of 4096. The charge LSB then becomes:

$$q_{LSB} = 0.34mAh \bullet \frac{50m\Omega}{R_{SENSE}} \bullet \frac{M}{4096}$$

APPLICATIONS INFORMATION

To use as much of the range of the accumulated charge register as possible the prescaler factor M should be chosen for a given battery capacity Q_{BAT} and a sense resistor R_{SENSE} as:

$$M \geq 4096 \bullet \frac{Q_{BAT}}{2^{16} \bullet 0.340mAh} \bullet \frac{R_{SENSE}}{50m\Omega}$$

M can be set to 1, 4, 16, ... 4096 by programming B[5:3] of the control register as $M = 2^{2 \bullet (4 \bullet B[5] + 2 \bullet B[4] + B[3])}$. The default value is 4096.

In the above example of a 100mAh battery and an R_{SENSE} of 50mΩ, the prescaler should be programmed to M = 64. The q_{LSB} is then 5313µAh and the battery capacity corresponds to roughly 18821 q_{LSB}s.

Figure 3 illustrates the best choice for prescaler value M and the sense resistor as function of the ratio between battery capacity (Q_{BAT}) and maximum current (I_{MAX}). It can be seen, that for high current applications with low battery capacity the prescaler value should be reduced, whereas in low current applications with a large battery the sense resistor should be reduced with respect to its default value of 50mV/I_{MAX}.

ADC Mode B[7:6]

The LTC2943 features an ADC which measures either voltage on SENSE⁻ (battery voltage), voltage difference between SENSE⁺ and SENSE⁻ (battery current) or temperature via an internal temperature sensor. The reference voltage and clock for the ADC are generated internally.

The ADC has four different modes of operation as shown in Table 3. These modes are controlled by bits B[7:6] of the control register. At power-up, bits B[7:6] are set to [00] and the ADC is in sleep mode.

A single conversion of the three measured quantities is initiated by setting the bit B[7:6] to [01]. After three conversions (voltage, current and temperature), the ADC resets B[7:6] to [00] and goes back to sleep.

The LTC2943 is set to scan mode by setting B[7:6] to [10]. In scan mode the ADC converts voltage, current, then temperature, then sleeps for approximately 10 seconds. It then reawakens automatically and repeats the three conversions. The chip remains in scan mode until reprogrammed by the host.

Programming B[7:6] to [11] sets the chip into automatic mode where the ADC continuously performs voltage, current and temperature conversions. The chip stays in automatic mode until reprogrammed by the host.

Programming B[7:6] to [00] puts the ADC to sleep. If control bits B[7:6] change within a conversion, the ADC will complete the running cycle of conversions before entering the newly selected mode.

A conversion of voltage requires 33ms (typical), and current and temperature conversions are completed in 4.5ms (typical). At the end of each conversion, the corresponding registers are updated. If the converted quantity exceeds the values programmed in the threshold registers, a flag is set in the status register and the $\overline{ALCC}$ pin is pulled low (if alert mode is enabled).

During ADC conversions additional currents are sunk from SENSE⁺ and SENSE⁻, refer to the Electrical Characteristics table for details.

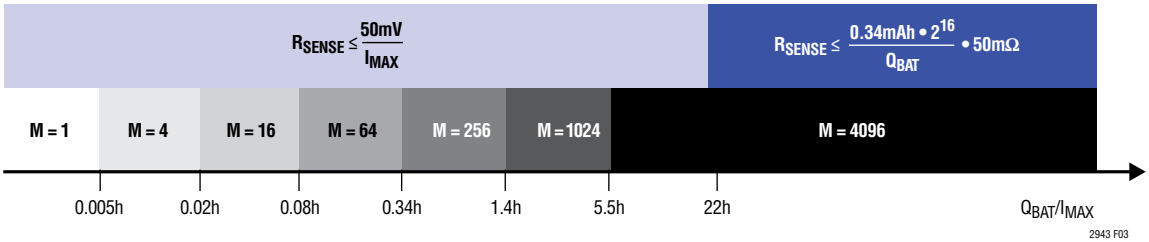


Figure 3. Choice of Sense Resistor and Prescaler as Function of Battery Capacity and Maximum Current

APPLICATIONS INFORMATION

Alert Thresholds Registers (E,F,G,H,K,L,M,N,Q,R,S,T,W,X)

For each of the measured quantities (battery charge, voltage, current and temperature) the LTC2943 features high and low threshold registers. At power-up, the high thresholds are set to FFFFh while the low thresholds are set to 0000h, with the effect of disabling them. All thresholds can be programmed to a desired value via I²C. As soon as a measured quantity exceeds the high threshold or falls below the low threshold, the LTC2943 sets the corresponding flag in the status register and pulls the $\overline{ALCC}$ pin low if alert mode is enabled via bits B[2:1].

Accumulated Charge Register (C,D)

The coulomb counting circuitry in the LTC2943 integrates current through the sense resistor. The result of this charge integration is stored in the 16-bit accumulated charge register (registers C, D). As the LTC2943 does not know the actual battery status at power-up, the accumulated charge register (ACR) is set to mid-scale (7FFFh). If the host knows the status of the battery, the accumulated charge (C[7:0]D[7:0]) can be either programmed to the correct value via I²C or it can be set after charging to FFFFh (full) by pulling the $\overline{ALCC}$ pin low if charge complete mode is enabled via bits B[2:1]. Note that before writing to the accumulated charge registers, the analog section should be temporarily shut down by setting B[0] to 1. In order to avoid a change in the accumulated charge registers between reading MSBs C[7:0] and LSBs D[7:0], it is recommended to read them sequentially as shown in Figure 10.

Voltage Registers (I,J), and Voltage Threshold Registers (K,L,M,N)

The result of the 14-bit ADC conversion of the voltage at SENSE⁻ is stored in the voltage registers (I, J).

From the result of the 16-bit voltage registers I[7:0]J[7:0] the measured voltage can be calculated as:

$$V_{SENSE^-} = 23.6V \bullet \frac{RESULT_h}{FFFF_h} = 23.6V \bullet \frac{RESULT_{DEC}}{65535}$$

Example 1: a register value I[7:0] = B0h and J[7:0] = 1Ch corresponds to a voltage on SENSE⁻ of:

$$V_{SENSE^-} = 23.6V \bullet \frac{B01C_h}{FFFF_h} = 23.6V \bullet \frac{45084_{DEC}}{65535} \approx 16.235V$$

Example 2: To set a low level threshold for the battery voltage of 7.2V, register M should be programmed to 4Eh and register N to 1Ah.

Current Registers (O,P) and Current Threshold Registers (Q,R,S,T)

The result of the current conversion is stored in the current registers (O,P).

As the ADC resolution is 12 bits in current mode, the lowest four bits of the combined current registers (O, P) are always zero.

The ADC measures battery current by converting the voltage, V_{SENSE}, across the sense resistor R_{SENSE}. Depending on whether the battery is being charged or discharged, the measured voltage drop on R_{SENSE} is positive or negative. The result is stored in registers O and P in excess –32767 representation. O[7:0] = FFh, P[7:0] = FFh corresponds to the full scale positive voltage 60mV. While O[7:0] = 00h, P[7:0] = 00h corresponds to the full scale negative voltage –60mV. The battery current can be obtained from the two byte register O[7:0]P[7:0] and the value of the chosen sense resistor R_{SENSE}:

$$I_{BAT} = \frac{V_{SENSE}}{R_{SENSE}} = \frac{60mV}{R_{SENSE}} \bullet \left(\frac{RESULT_h - 7FFF_h}{7FFF_h}\right) = \frac{60mV}{R_{SENSE}} \bullet \left(\frac{RESULT_{DEC} - 32767}{32767}\right)$$

Positive current is measured when the battery is charging and negative current is measured when the battery is discharging.

APPLICATIONS INFORMATION

Example 1: a register value of O[7:0] = A8h P[7:0] = 40h together with a sense resistor $R_{SENSE} = 50m\Omega$ corresponds to a battery current:

$$I_{BAT} = \frac{60mV}{50m\Omega} \bullet \left(\frac{A840_h - 7FFF_h}{7FFF_h} \right) =$$

$$\frac{60mV}{50m\Omega} \bullet \left(\frac{43072 - 32767}{32767} \right) \approx 377.3mA$$

The positive current result indicates that the battery is being charged.

The values in the threshold register for the current mode Q,R,S,T are also expressed in excess –32767 representation in the same manner as the current conversion result. The alert after a current measurement is set if the result is higher than the value stored in the high threshold registers Q,R or lower than the value stored in the low value registers S,T.

Example 2: In an application, the user wants to get an alert if the absolute current through the sense resistor, R_{SENSE}, of 50mΩ exceeds 1A. This is achieved by setting the upper threshold I_{HIGH} in register [Q,R] to 1A and the lower threshold I_{LOW} in register [S,T] to –1A. The formula for I_{BAT} leads to:

$$I_{HIGH(DEC)} = \left(\frac{1A \bullet 50m\Omega}{60mV} \bullet 32767 \right) + 32767 = 60073$$

$$I_{LOW(DEC)} = \left(\frac{-1A \bullet 50m\Omega}{60mV} \bullet 32767 \right) + 32767 = 5461$$

Leading the user to set Q[7:0] = EAh, R[7:0] = A9h for the high threshold and S[7:0] = 15h and T[7:0] = 55h for the low threshold.

Temperature Registers (U,V), and Temperature Threshold Registers (W,X)

As the ADC resolution is 11 bits in temperature mode, the lowest five bits of the combined temperature registers (U, V) are always zero.

The actual temperature can be obtained from the two byte register U[7:0]V[7:0] by:

$$T = 510K \bullet \frac{RESULT_h}{FFFF_h} = 510K \bullet \frac{RESULT_{DEC}}{65535}$$

Example: a register value of U[7:0] = 96h, V[7:0] = 96h corresponds to ~300K or ~27°C

A high temperature limit of 60°C is programmed by setting register W to A7h. Note that the temperature threshold register is a single byte register and only the eight MSBs of the 11 bits temperature result are checked.

Effect of Differential Offset Voltage on Total Charge Error

In battery gas gauges, an important parameter is the differential offset (V_{OS}) of the circuitry monitoring the battery charge. Many coulomb counter devices perform an analog to digital conversion of V_{SENSE}, where V_{SENSE} is the voltage drop across the sense resistor, and accumulate the conversion results to infer charge. In such an architecture, the differential offset V_{OS} causes relative charge error of V_{OS}/V_{SENSE}. For small V_{SENSE} values V_{OS} can be the main source of error.

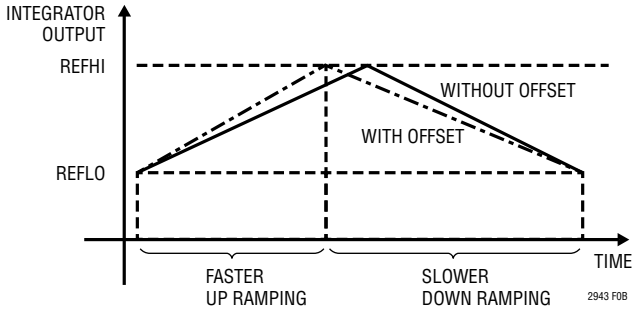
The LTC2943 performs the tracking of the charge with an analog integrator. This approach allows to continuously monitor the battery charge and significantly lowers the error due to differential offset. The relative charge error due to offset (CE_{OV}) can be expressed by:

$$CE_{OV} = \left(\frac{V_{OS}}{V_{SENSE}} \right)^2$$

As example, at a 1mV input signal, a differential voltage offset V_{OS} = 20µV results in a 2% error using digital integration, whereas the error is only 0.04% (a factor of 50 times smaller!) using the analog integration approach of LTC2943.

APPLICATIONS INFORMATION

The reduction of the impact of the offset in LTC2943 can be explained by its integration scheme depicted in Figure 2. While positive offset accelerates the up ramping of the integrator output from REFLO to REFHI, it slows the down ramping from REFHI to REFLO thus the effect is largely canceled as depicted below.



For input signals with an absolute value smaller than the offset of the internal op amp, the LTC2943 stops integrating and does not integrate its own offset.

I²C/SMBus Interface

The LTC2943 communicates with a bus master using a 2-wire interface compatible with I²C and SMBus. The 7-bit hard coded I²C address of the LTC2943 is 1100100.

The LTC2943 is a slave only device. The serial clock line (SCL) is input only while the serial data line (SDA) is bidirectional. The device supports I²C standard and fast mode. For more details refer to the I²C Protocol section.

I²C Protocol

The LTC2943 uses an I²C/SMBus-compatible 2-wire interface supporting multiple devices on a single bus. Connected devices can only pull the bus lines low and must never drive the bus high. The bus wires are externally connected to a positive supply voltage via current sources or pull-up resistors. When the bus is idle, all bus lines are high. Data on the I²C bus can be transferred at rates of up to 100kbit/s in standard mode and up to 400kbit/s in fast mode.

Each device on the I²C/SMbus is recognized by a unique address stored in that device and can operate as either a transmitter or receiver, depending on the function of the device. In addition to transmitters and receivers, devices can also be classified as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At the same time any device addressed is considered a slave. The LTC2943 always acts as a slave.

Figure 4 shows an overview of the data transmission on the I²C bus.

Start and Stop Conditions

When the bus is idle, both SCL and SDA must be high. A bus master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP condition by

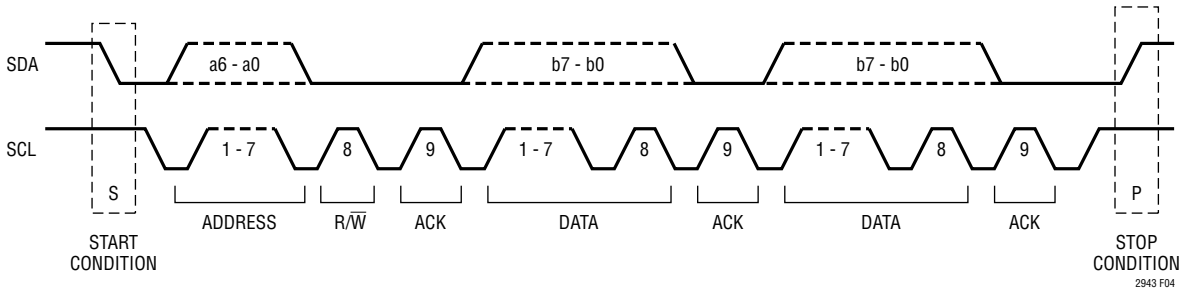


Figure 4. Data Transfer Over I²C or SMBus

APPLICATIONS INFORMATION

transitioning SDA from low to high while SCL is high. The bus is then free for another transmission. When the bus is in use, it stays busy if a repeated START (Sr) is generated instead of a STOP condition. The repeated START (Sr) conditions are functionally identical to the START (S).

Write Protocol

The master begins a write operation with a START condition followed by the seven bit slave address 1100100 and the R/W bit set to zero, as shown in Figure 5. The LTC2943 acknowledges this by pulling SDA low and the master sends a command byte which indicates which internal register the master is to write. The LTC2943 acknowledges and latches the command byte into its internal register address pointer. The master delivers the data byte, the LTC2943 acknowledges once more and latches the data into the desired register. The transmission is ended when the master sends a STOP condition. If the master continues by sending a second data byte instead of a stop, the LTC2943 acknowledges again, increments its address pointer and latches the second data byte in the following register, as shown in Figure 6.

S	ADDRESS	$\overline{W}$	A	REGISTER	A	DATA	A	P
	1100100	0	0	01h	0	FCh	0	

2943 F05

FROM MASTER TO SLAVE

FROM SLAVE TO MASTER

A: ACKNOWLEDGE (LOW)
$\overline{A}$: NOT ACKNOWLEDGE (HIGH)
S: START CONDITION
P: STOP CONDITION
R: READ BIT (HIGH)
$\overline{W}$: WRITE BIT (LOW)

Figure 5. Writing FCh to the LTC2943 Control Register (B)

S	ADDRESS	$\overline{W}$	A	REGISTER	A	DATA	A	DATA	A	P
	1100100	0	0	02h	0	F0h	0	01h	0	

2943 F06

Figure 6. Writing F001h to the LTC2943 Accumulated Charge Register (C, D)

Read Protocol

The master begins a read operation with a START condition followed by the seven bit slave address 1100100 and the R/W bit set to zero, as shown in Figure 7. The LTC2943 acknowledges and the master sends a command byte which indicates which internal register the master is to read. The LTC2943 acknowledges and then latches the command byte into its internal register address pointer. The master then sends a repeated START condition followed by the same seven bit address with the R/W bit now set to one. The LTC2943 acknowledges and sends the contents of the requested register. The transmission is ended when the master sends a STOP condition. If the master acknowledges the transmitted data byte, the LTC2943 increments its address pointer and sends the contents of the following register as depicted in Figure 8.

S	ADDRESS	$\overline{W}$	A	REGISTER	A	Sr	ADDRESS	R	A	DATA	$\overline{A}$	P
	1100100	0	0	00h	0		1100100	1	0	01h	1	

2943 F07

Figure 7. Reading the LTC2943 Status Register (A)

S	ADDRESS	$\overline{W}$	A	REGISTER	A	Sr	ADDRESS	R	A	DATA	A	DATA	$\overline{A}$	P
	1100100	0	0	08h	0		1100100	1	0	F1h	0	24h	1	

2943 F08

Figure 8. Reading the LTC2943 Voltage Register (I, J)

APPLICATIONS INFORMATION

Alert Response Protocol

In a system where several slaves share a common interrupt line, the master can use the alert response address (ARA) to determine which device initiated the interrupt (Figure 9).

S	ALERT RESPONSE ADDRESS	R	A	DEVICE ADDRESS	$\overline{A}$	P
	0001100	1	0	1100100	1	

2943 F09

Figure 9. LTC2943 Serial Bus SDA Alert Response Protocol

S	ADDRESS	$\overline{W}$	A	REGISTER	A	S	ADDRESS	R	A	DATA	A	DATA	$\overline{A}$	P
	1100100	0	0	02h	0		1100100	1	0	80h	0	01h	1	

2943 F10

Figure 10. Reading the LTC2943 Accumulated Charge Registers (C, D)

S	ADDRESS	$\overline{W}$	A	REGISTER	A	DATA	P
	1100100	0	0	01h	0	4C	

40ms

S	ADDRESS	$\overline{W}$	A	REGISTER	A	S	ADDRESS	R	A	DATA	A	DATA	$\overline{A}$	P
	1100100	0	0	08h	0		1100100	1	0	F1h	0	80h	1	

2943 F11

Figure 11. ADC Single Conversion Sequence and Reading of Voltage Registers (I,J)

The master initiates the ARA procedure with a START condition and the special 7-bit ARA bus address (0001100) followed by the read bit (R) = 1. If the LTC2943 is asserting the $\overline{ALCC}$ pin in alert mode, it acknowledges and responds by sending its 7-bit bus address (1100100) and a 1. While it is sending its address, it monitors the SDA pin to see if another device is sending an address at the same time using standard I^2C bus arbitration. If the LTC2943 is sending a 1 and reads a 0 on the SDA pin on the rising edge of SCL, it assumes another device with a lower address is sending and the LTC2943 immediately aborts its transfer and waits for the next ARA cycle to try again. If transfer is successfully completed, the LTC2943 will stop pulling down the $\overline{ALCC}$ pin and will not respond to further ARA requests until a new Alert event occurs.

PC Board Layout Suggestions

Keep all traces as short as possible to minimize noise and inaccuracy. Use a 4-wire Kelvin sense connection for the sense resistor, locating the LTC2943 close to the resistor with short sense-traces to the $SENSE^+$ and $SENSE^-$ pins. Use wider traces from the resistor to the battery, load and/or charger. Put the bypass capacitor close to $SENSE^+$ and GND.

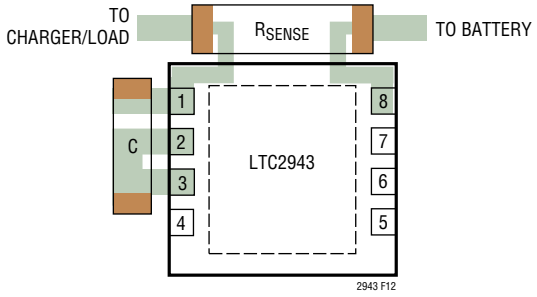
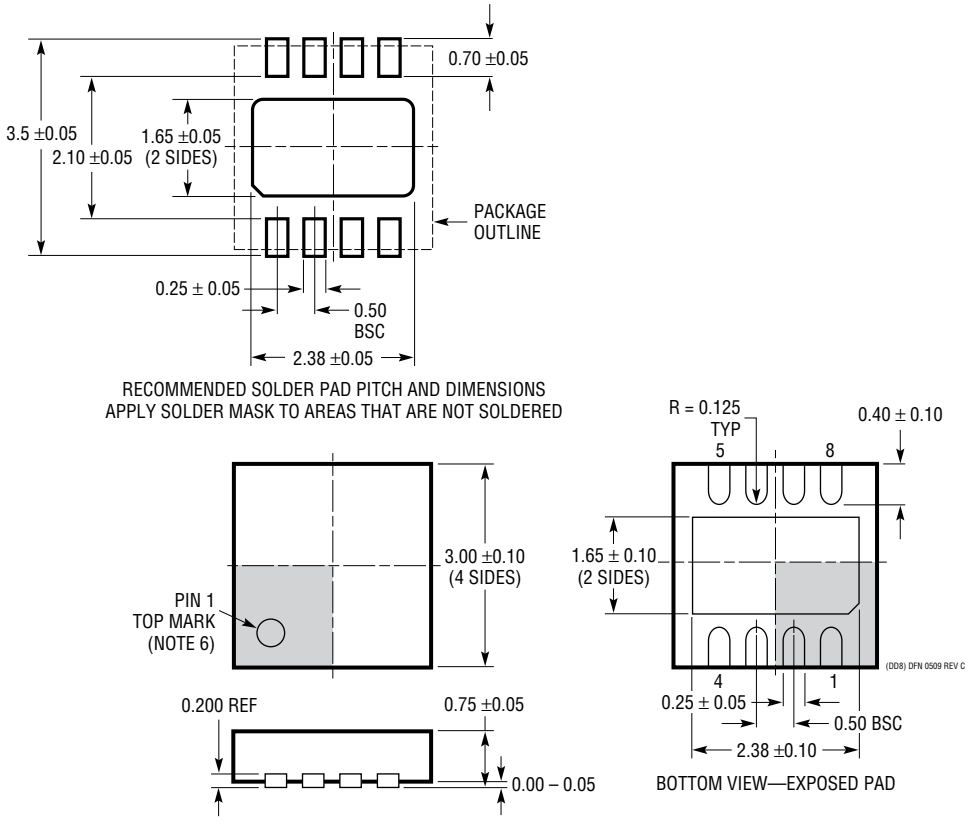


Figure 12. Kelvin Connection on Sense Resistor

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698 Rev C)

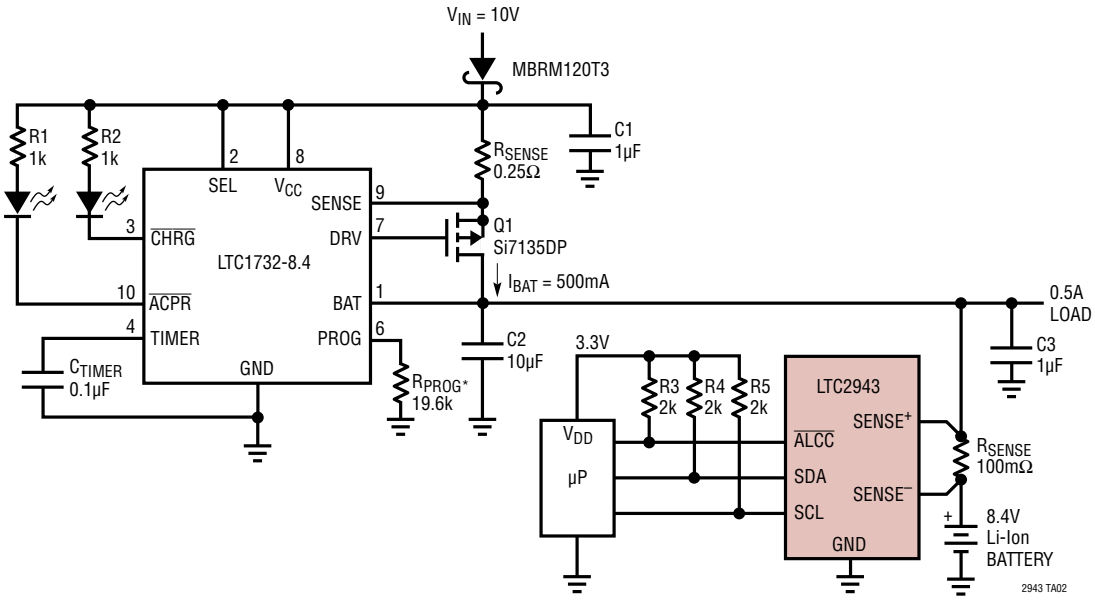


NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

2-Cell 8.4V Linear Charger and Battery Gas Gauge



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Battery Gas Gauges		
LTC2941	Battery Gas Gauge with I²C Interface	2.7V to 5.5V Operation, 6-Lead (2mm × 3mm) DFN Package
LTC2941-1	1A I²C Battery Gas Gauge with Internal Sense Resistor	2.7V to 5.5V Operation, 6-Lead (2mm × 3mm) DFN Package
LTC2942	Battery Gas Gauge with Temperature/Voltage Measurement	2.7V to 5.5V Operation, 14-Bit ΔΣ-ADC, 6-Lead (2mm × 3mm) DFN Package
LTC2942-1	1A Battery Gas Gauge with Internal Sense Resistor and Temperature/Voltage Measurement	2.7V to 5.5V Operation, 14-Bit ΔΣ-ADC, 6-Lead (2mm × 3mm) DFN Package
LTC4150	Coulomb Counter/Battery Gas Gauge	2.7V to 8.5V Operation, 10-Pin MSOP Package
Battery Chargers		
LTC4000	High Voltage High Current Controller for Battery Charging and Power Management	3V to 60V Operation, 28-Lead (4mm × 5mm) QFN or SSOP Packages
LTC4009	High Efficiency, Multi-Chemistry Battery Charger	6V to 28V Operation, 20-Lead (4mm × 4mm) QFN Package
LTC4012	High Efficiency, Multi-Chemistry Battery Charger with PowerPath™ Control	6V to 28V Operation, 20-Lead (4mm × 4mm) QFN Package
LT3652HV	Power Tracking 2A Battery Charger	Input Supply Voltage Regulation Loop for Peak Power Tracking, 5V to 34V Operation, 1MHz, 2A Charge Current, 3mm × 3mm DFN-12 and MSOP-12 Packages
LTC1732	Li-Ion Battery Charger	4.5V to 12V Operation, MSOP-10 Package

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